CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being transmitted to Examiner Ilwoo PARK via the USPTO EFS-Web on **May 4, 2006.**

Jinny Nguyen

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	Date: May 4, 2006
Phuc Ky DO, et al.	Confirmation No. 8869
Serial No: 10/671,981	Group Art Unit: 2182
Filed: September 25, 2003	Examiner: Ilwoo PARK

For: METHOD AND SYSTEM FOR AUTOMATICALLY DETERMINING I/O CONNECTOR CONFIGURATION

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

Dear Sir or Madam:

Appellant submits this Appeal Brief pursuant to the Notice of Appeal filed in this case on March 6, 2005.

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corp. of Armonk, New York by virtue of an assignment from the inventor(s) recorded in the U.S. Patent and Trademark Office on September 25, 2003, at Reel No. 014553, Frame No. 0437.

II. RELATED APPEALS AND INTERFERENCES

There are no appeals, interferences, or judicial proceedings known to Appellant, the Appellant's legal representative, or Assignee, which may be related to, directly affect, be directly affected by, or have a bearing on the decision by the Board of Patent Appeals and Interferences in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-15 have been rejected. Appeal is taken from the rejection of claims 1-15.

IV. STATUS OF AMENDMENTS

No amendments were filed subsequent to the final Office action dated December 7, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 recites a method for automatically determining a configuration of an I/O connector panel. The method includes providing information about the capabilities of the I/O connector panel (12) to a memory (202) within the I/O connector panel (12) (102). *See, e.g.*, pg. 3, lns. 17-21; pg. 3, ln. 23 to pg. 4, ln. 2; pg. 4, lns. 8-9; pg. 6, lns. 3-11; Figs. 1-3. The method also includes examining the information in the memory (202) (104). *See, e.g.*, pg. 4, lns. 2 and 6-8; pg. 6, lns. 9-11; Figs. 2-3. The method further includes downloading at least one driver to a system coupled to the I/O connector panel (12) based upon the examined information (106). *See, e.g.*, pg. 4, lns. 2-4 and 9-11; Figs. 2-3.

Independent claim 5 recites an I/O connector panel. The I/O connector panel (12) includes a plurality of I/O connectors (204). *See, e.g.*, pg. 3, lns. 18-19; pg. 5, lns. 20-21; pg. 6, lns. 7-9, 13-14, and 17-18; Fig. 2. The I/O connector panel (12) also includes a memory (202) containing information about the capabilities of the I/O connector panel (12), wherein, when the memory (202) is examined, at least one driver can be downloaded to a system coupled to the I/O connector panel (12). *See, e.g.*, pg. 3, lns. 17-21; pg. 3, ln. 23 to pg. 4, ln. 4; pg. 4, lns. 6-11; pg. 6, lns. 3-11; Figs. 2-3.

Independent claim 10 recites a processing system. The processing system includes a core PC function (10). *See, e.g.*, pg. 3, lns. 7-10; pg. 4, lns. 9-11 and 15-21; Fig. 1. The processing system also includes at least one I/O connector panel (12) coupled to the core PC function (10). *See, e.g.*, pg. 3, lns. 9-10; pg. 4, lns. 8-11 and 15-17; Fig. 1. The at least one I/O connector panel (12) includes a plurality of I/O connectors (204). *See, e.g.*, pg. 3, lns. 18-19; pg. 5, lns. 20-21; pg. 6, lns. 7-9, 13-14, and 17-18; Fig. 2. In addition, the at least one I/O connector panel (12) includes a memory (202) containing information about the capabilities of the I/O connector panel (12), wherein, when the memory (202) is examined, at least one driver can be downloaded to a system coupled to the I/O connector panel (12). *See, e.g.*, pg. 3, lns. 17-21; pg. 3, ln. 23 to pg. 4, ln. 4; pg. 4, lns. 6-11; pg. 6, lns. 3-11; Figs. 2-3.

Independent claim 14 recites a processing system. The processing system includes a core PC function (10). *See, e.g.*, pg. 3, lns. 7-10; pg. 4, lns. 9-11 and 15-21; Fig. 1. The processing system also includes a plurality of I/O connector panels (12a, 12b) coupled to the core PC function (10). *See, e.g.*, pg. 3, lns. 9-10; pg. 4, lns. 8-11 and 15-17; Fig. 1. Each of the plurality of I/O connector panels (12) includes a plurality of I/O connectors (204). *See, e.g.*, pg. 3, lns.

18-19; pg. 5, lns. 20-21; pg. 6, lns. 7-9, 13-14, and 17-18; Fig. 2. Additionally, each of the plurality of I/O connector panels (12) includes an EEROM (202) containing information about the capabilities of the I/O connector panel (12), wherein, when the memory (202) is examined, at least one driver can be downloaded to a system coupled to the I/O connector panel (12). *See, e.g.*, pg. 3, lns. 17-21; pg. 3, ln. 23 to pg. 4, ln. 4; pg. 4, lns. 6-11; pg. 6, lns. 3-11; Figs. 2-3. Furthermore, each of the plurality of I/O connector panels (12) includes connector logic (206) coupled to the EEROM (202) for I/O distribution. *See, e.g.*, pg. 3, lns. 12-16 and 19-21; Fig. 2.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Appellant requests review as to claims 1, 3-5, 7-10, and 12-13 and their rejection under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 6,668,376 to Wang et al. (hereinafter "Wang").

2. Appellant requests review as to claims 1, 3-5, 7-10, and 12-13 and their rejection under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. Pub. No. 2003/0182414 to O'Neill (hereinafter "O'Neill").

3. Appellant requests review as to claims 2, 6, 11, and 14-15 and their rejection under 35 U.S.C. § 103(a) as being unpatentable over Wang in view of Japanese Pat. Pub. No. 2001-117835 to Shinohara et al. (hereinafter "Shinohara").

4. Appellant requests review as to claims 2, 6, 11, and 14-15 and their rejection under 35 U.S.C. § 103(a) as being unpatentable over O'Neill in view of what is well known in the art.

VII. ARGUMENTS

1. Claims 1, 3-5, 7-10, and 12-13 Are Not Properly Rejected Under 35 U.S.C. § 102(e) as Being Anticipated By Wang

Claim 1 recites a method for automatically determining a configuration of an I/O connector panel. The method includes providing information about the capabilities of the I/O connector panel to a memory within the I/O connector panel, examining the information in the memory, and downloading at least one driver to a system coupled to the I/O connector panel based upon the examined information.

Wang does not disclose, teach, or suggest the claimed subject matter.

Wang is directed to "a system and method which automatically locates and loads a device driver in a computer for a peripheral device attached to the computer" (col. 1, lns. 9-11 of Wang). In Wang, when a peripheral device is connected to a computer, "the peripheral device provides unique identification data to the computer to which it is connected. The computer then obtains a URL address, which the manufacturer of the peripheral device previously set up to contain the device driver corresponding to the peripheral device, based on the obtained identification data from the peripheral device. Then, the obtained URL address containing the device driver for the peripheral device is accessed. The device driver is then downloaded from the accessed URL address and installed in the computer" (col. 2, lns. 28-37 of Wang). To obtain the URL address, Wang teaches that either "the peripheral device itself provides the URL address data within its identification data provided to the computer" or "the computer contains a database at least correlating different identification data to URL addresses" (col. 2, lns. 45-49 of Wang).

(A)(i) Wang does not disclose, teach, or suggest "providing information about the capabilities of the I/O connector panel to a memory within the I/O connector panel"

Wang does not disclose, teach, or suggest "providing information about the capabilities of the I/O connector panel to a memory within the I/O connector panel," as recited in claim 1. In the final Office action, the Examiner states:

> Wang et al teach . . . providing information [URL database associated with peripheral device identification data in col. 3, line 61 to col. 4, line 4] about the capabilities [peripheral device identification data including a model, a type, and/or a description of the peripheral device to be attached to a connector; fig. 2; col. 4, lines 30-60] of the I/O connector panel to a memory [URL database 13 in fig. 2] within the I/O connector panel . . . .

(December 7, 2005 final Office action, pg. 2).

The Examiner also asserts:

> Wang provides URL database (information) stored in URL database 13 in computer 1 providing a plurality of I/O connectors; the URL database information is associated with peripheral device identification data including a model, a type, and/or a description of the peripheral device to be attached to a connector.

(December 7, 2005 final Office action, pg. 9).

Based on the Examiner's comments, it appears that the Examiner is construing "the I/O connector panel" recited in claim 1 to be a computer. Although the Examiner is entitled to a reasonably broad interpretation of the claim terms, the Examiner cannot select an interpretation that is contrary to the accepted meaning of a term by those of ordinary skill in the art. "The broadest reasonable interpretation of the claims must . . . be consistent with the interpretation that those skilled in the art would reach," MPEP § 2111, citing *In re Cortright*, 165 F.3d 1353, 1359, 49 USPQ2d 1464, 1468 (Fed. Cir. 1999).

For the Examiner to argue that the "I/O connector panel" recited in claim 1 corresponds to Wang's "computer 1" is simply inconsistent with the interpretation that those skilled in the art would reach. In addition, claim 1 specifically recites "downloading at least one driver to a system coupled to the I/O connector panel," which clearly distinguishes a "system" from an "I/O connector panel" that is coupled thereto. Hence, "computer 1" in Wang cannot be construed as disclosing the "I/O connector panel" recited in claim 1.

Although Wang does disclose a local port 11 to which a peripheral device 2 is connected, Wang does not disclose "a memory within the I/O connector panel," as recited in claim 1. In particular, as illustrated in Figure 2 of Wang, URL database 13, which the Examiner has construed as disclosing the "memory" recited in claim 1, is completely separate from local port 11. Further, it is not inherent that URL database 13 is within local port 11 because Wang specifically states that even though "URL database 13 . . . [is] shown in FIG. [2] as a part of the computer 1, . . . [it] can also be an external database" (col. 3, lns. 61-63 of Wang). Thus, "URL database 13" in Wang cannot be construed as disclosing "a memory within the I/O connector panel" recited in claim 1.

Therefore, Wang fails to disclose, teach, or suggest "providing information about the capabilities of the I/O connector panel to a memory within the I/O connector panel," as recited in claim 1.

(A)(ii) The Examiner has not established anticipation under 35 U.S.C. § 102

Anticipation under 35 U.S.C. § 102 requires the disclosure in a single piece of prior art of each and every limitation of a claimed invention. (*See, e.g.*, Electro Med. Sys. S.A. v. Cooper

Life Sciences, 34 F.3d 1048, 32 U.S.P.Q.2d 1017, 1019 (Fed. Cir. 1994)). The Examiner has failed to show that the element discussed in section (A)(i) above is disclosed in Wang.

Therefore, claim 1 is improperly rejected under 35 U.S.C. § 102(e) as being anticipated by Wang. Claims 3-4 depend from claim 1 and are therefore improperly rejected for at least the same reasons. Claims 5 and 10 each recites elements similar to those of claim 1 and are therefore improperly rejected for at least the same reasons. Claims 7-9 and 12-13 depend from claims 5 and 10, respectively, and are therefore improperly rejected for at least the same reasons.

2. Claims 1, 3-5, 7-10, and 12-13 Are Not Properly Rejected Under 35 U.S.C. § 102(e) as Being Anticipated By O'Neill

Claim 1 recites a method for automatically determining a configuration of an I/O connector panel. The method includes providing information about the capabilities of the I/O connector panel to a memory within the I/O connector panel, examining the information in the memory, and downloading at least one driver to a system coupled to the I/O connector panel based upon the examined information.

O'Neill does not disclose, teach, or suggest the claimed subject matter.

O'Neill is directed to "a software system and method for updating information which reduces the size of an update and distributes the update in a platform independent manner" (pg. 1, para. 0002 of O'Neill). In O'Neill, "an update generator . . . identifies differences between the updated operating code and the resident operating code and thereafter generates an update package comprising an instruction set which specifies how to generate the updated operating code utilizing at least a portion of . . . the resident operating code" (pg. 2, para. 0013 of O'Neill).

The update package is then distributed "to the electronic devices . . . and . . . executed by the client modules" residing thereon (pg. 2, para. 0013 of O'Neill).

(B)(i) O'Neill does not disclose, teach, or suggest "providing information about the capabilities of the I/O connector panel to a memory within the I/O connector panel"

O'Neill does not disclose, teach, or suggest "providing information about the capabilities of the I/O connector panel to a memory within the I/O connector panel," as recited in claim 1. In the final Office action, the Examiner states:

> O'Neill teaches . . . providing information [server manifest in paragraphs 0048, 0057] about the capabilities [server manifest having a list or version information describing available update packages which pertain to a wide range of particular client devices attached to the update server array in paragraph 0048] of the I/O connector panel to a memory [onboard memory in paragraph 0063] within the I/O connector panel . . . .

(December 7, 2005 final Office action, pg. 4).

The Examiner also asserts:

> O'Neill provides a server manifest (information) stored in on board memory retained by the update server 136 in the update server array (I/O connector panel) providing a plurality of I/O connectors to connect a plurality of clients; the server manifest information having a list or version information describing available update packages which pertain to a wide range of particular client devices attached to the update server array.

(December 7, 2005 final Office action, pg. 9).

As discussed above in section (A)(i), claim terms cannot be construed so broadly as to be contrary to the interpretation that would be given by those skilled in the art. *See, e.g.*, MPEP § 2111. Just as those skilled in the art will readily recognize that an "I/O connector panel" is not a "computer," they will also readily recognize that an "I/O connector panel" is not a "server" or a

"server array," as asserted by the Examiner. In addition, as noted above in section (A)(i), claim 1 specifically distinguishes between an "I/O connector panel" and a "system" in which it is coupled to. Thus, "server 136" and "server array 142" in O'Neill cannot be construed as disclosing the "I/O connector panel" recited in claim 1.

Since "server 136" and "server array 142" in O'Neill cannot be construed as disclosing the "I/O connector panel" recited in claim 1, O'Neill also fails to disclose "a memory within the I/O connector panel," as recited in claim 1, because the "onboard memory or storage component" in server 136 cited by the Examiner cannot be construed as disclosing "a memory within the I/O connector panel."

Further, the "server manifest" in O'Neill cannot be construed as disclosing "information about the capabilities of the I/O connector panel," as recited in claim 1, since "server 136" cannot be construed as disclosing the "I/O connector panel" and the server manifest only contains "information used to determine the latest available version of the software, file system, or hardware to be updated" (pg. 7, para. 0063 of O'Neill).

Therefore, O'Neill, like Wang, fails to disclose, teach, or suggest "providing information about the capabilities of the I/O connector panel to a memory within the I/O connector panel," as recited in claim 1.

(B)(ii) The Examiner has not established anticipation under 35 U.S.C. § 102

Anticipation under 35 U.S.C. § 102 requires the disclosure in a single piece of prior art of each and every limitation of a claimed invention. (*See, e.g.*, Electro Med. Sys. S.A. v. Cooper

Life Sciences, 34 F.3d 1048, 32 U.S.P.Q.2d 1017, 1019 (Fed. Cir. 1994)). The Examiner has failed to show that the element discussed in section (B)(i) above is disclosed in O'Neill.

Therefore, claim 1 is improperly rejected under 35 U.S.C. § 102(e) as being anticipated by O'Neill. Claims 3-4 depend from claim 1 and are therefore improperly rejected for at least the same reasons. Claims 5 and 10 each recites elements similar to those of claim 1 and are therefore improperly rejected for at least the same reasons. Claims 7-9 and 12-13 depend from claims 5 and 10, respectively, and are therefore improperly rejected for at least the same reasons.

3. Claims 2, 6, 11, and 14-15 Are Not Properly Rejected Under 35 U.S.C. § 103(a) as Being Unpatentable Over Wang in View of Shinohara

(C) Claims 2, 6, and 11

Claim 2 depends from claim 1 and recites wherein the memory comprises an EEROM.

Wang and Shinohara do not, alone or in combination, disclose, teach, or suggest the claimed subject matter.

Wang is directed to "a system and method which automatically locates and loads a device driver in a computer for a peripheral device attached to the computer" (col. 1, lns. 9-11 of Wang). In Wang, when a peripheral device is connected to a computer, "the peripheral device provides unique identification data to the computer to which it is connected. The computer then obtains a URL address, which the manufacturer of the peripheral device previously set up to contain the device driver corresponding to the peripheral device, based on the obtained identification data from the peripheral device. Then, the obtained URL address containing the device driver for the peripheral device is accessed. The device driver is then downloaded from the accessed URL

address and installed in the computer" (col. 2, lns. 28-37 of Wang). To obtain the URL address, Wang teaches that either "the peripheral device itself provides the URL address data within its identification data provided to the computer" or "the computer contains a database at least correlating different identification data to URL addresses" (col. 2, lns. 45-49 of Wang).

Shinohara is directed to a "printer, information system, and control information installing method" (Title). In Shinohara, "[a] printer 10 which can be connected to a user host connected to a LAN 210 is equipped with a network interface card 110 for communicating with the user host, a flash ROM 118 stored with a URL indicating the location of driver software executed by the user host to control the printer 101, and a CPU 120 which sends the URL to the user host at a request from the user host. The user host is able to download the driver software by accessing the URL through the Internet" (Abstract).

(C)(i) Shinohara does not cure the deficiencies of Wang

Claim 2 depends from claim 1 and incorporates the limitations of that claim. As discussed above in Section (A)(i), Wang does not disclose, teach or suggest "providing information about the capabilities of the I/O connector panel to a memory within the I/O connector panel," as recited in claim 1.

Shinohara does not cure the deficiencies of Wang. In particular, Shinohara fails to disclose, teach, or suggest, and the Examiner has not cited any passage of Shinohara as disclosing, teaching, or suggesting, "providing information about the capabilities of the I/O connector panel to a memory within the I/O connector panel," as recited in claim 1.

Therefore, even if Wang and Shinohara were combined, the combination would neither teach nor suggest "providing information about the capabilities of the I/O connector panel to a memory within the I/O connector panel," as recited in claim 1.

(C)(ii) The Examiner has not established a *prima facie* case of obviousness

To establish a *prima facie* case of obviousness, the Examiner must make three basic showings. First, there must be some suggestion or motivation, either in the references or in the prior knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. (*See, e.g.*, In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Since the Examiner has failed to make the three basic showings, no *prima facie* case of obviousness has been established. Thus, claim 2 is improperly rejected under § 103(a) as being unpatentable over Wang in view of Shinohara. Claims 6 and 11 each incorporates the features of claim 2 and are therefore improperly rejected for at least the same reasons.

(D) Claims 14-15

Claim 14 recites a processing system that includes a core PC function and a plurality of I/O connector panels coupled to the core PC function, each of the plurality of I/O connector panels comprising a plurality of I/O connectors, an EEROM containing information about the capabilities of the I/O connector panel, wherein, when the memory is examined, at least one

driver can be downloaded to a system coupled to the I/O connector panel, and connector logic coupled to the EEROM for I/O distribution.

Wang and Shinohara do not, alone or in combination, disclose, teach, or suggest the claimed subject matter.

Wang is directed to "a system and method which automatically locates and loads a device driver in a computer for a peripheral device attached to the computer" (col. 1, lns. 9-11 of Wang). In Wang, when a peripheral device is connected to a computer, "the peripheral device provides unique identification data to the computer to which it is connected. The computer then obtains a URL address, which the manufacturer of the peripheral device previously set up to contain the device driver corresponding to the peripheral device, based on the obtained identification data from the peripheral device. Then, the obtained URL address containing the device driver for the peripheral device is accessed. The device driver is then downloaded from the accessed URL address and installed in the computer" (col. 2, lns. 28-37 of Wang). To obtain the URL address, Wang teaches that either "the peripheral device itself provides the URL address data within its identification data provided to the computer" or "the computer contains a database at least correlating different identification data to URL addresses" (col. 2, lns. 45-49 of Wang).

Shinohara is directed to a "printer, information system, and control information installing method" (Title). In Shinohara, "[a] printer 10 which can be connected to a user host connected to a LAN 210 is equipped with a network interface card 110 for communicating with the user host, a flash ROM 118 stored with a URL indicating the location of driver software executed by the user host to control the printer 101, and a CPU 120 which sends the URL to the user host at a

request from the user host. The user host is able to download the driver software by accessing the URL through the Internet" (Abstract).

(D)(i) Wang does not disclose, teach, or suggest "each of the plurality of I/O connector panels comprising . . . an EEROM containing information about the capabilities of the I/O connector panel"

Wang does not disclose, teach, or suggest "each of the plurality of I/O connector panels comprising . . . an EEROM containing information about the capabilities of the I/O connector panel," as recited in claim 14. In the final Office action, the Examiner states:

> Wang et al teach . . . a plurality of I/O connector panels coupled to the core PC function, each of the plurality of I/O connector panels comprising a plurality of I/O connectors [col. 1, lines 13-16], a memory containing information [URL database 13 in fig. 2, col. 3, line 61-col. 4, line 4] about the capabilities [peripheral device identification data including a model, a type, and/or a description of the peripheral device to be attached to a connector; fig. 2; col. 4, lines 30-60] of the I/O connector panel . . . .

(December 7, 2005 final Office action, pgs. 6-7).

As discussed above in sections (A)(i) and (B)(i), claim terms cannot be construed so broadly as to be inconsistent with the interpretation that would be reached by those skilled in the art. *See, e.g.*, MPEP § 2111. Appellant submits that those skilled in the art will readily recognize that an "I/O connector panel" is not a "computer," as asserted by the Examiner. In addition, claim 14 specifically recites that the "I/O connector panel" is coupled to a "core PC function" and a "system," thereby distinguishing an "I/O connector panel" from a "system" and a "core PC function." Hence, "computer 1" in Wang cannot be construed as disclosing the "I/O connector panel" recited in claim 14.

Further, as noted in section (A)(i) above, "URL database 13" in Wang cannot be construed as disclosing the "EEROM" in the "I/O connector panel," as recited in claim 14, because "URL database 13" is illustrated and described as being completely separate from "local port 11" and Wang expressly states that "URL database 13" does not even have to be located within "computer 1."

Therefore, Wang fails to disclose, teach, or suggest "each of the plurality of I/O connector panels comprising . . . an EEROM containing information about the capabilities of the I/O connector panel," as recited in claim 14.

(D)(ii) Shinohara does not cure the deficiencies of Wang

Shinohara does not cure the deficiencies of Wang. In particular, Shinohara fails to disclose, teach, or suggest, and the Examiner has not cited any passage of Shinohara as disclosing, teaching, or suggesting, "each of the plurality of I/O connector panels comprising . . . an EEROM containing information about the capabilities of the I/O connector panel," as recited in claim 14.

Therefore, even if Wang and Shinohara were combined, the combination would neither teach nor suggest "each of the plurality of I/O connector panels comprising . . . an EEROM containing information about the capabilities of the I/O connector panel," as recited in claim 14.

(D)(iii) The Examiner has not established a *prima facie* case of obviousness

To establish a *prima facie* case of obviousness, the Examiner must make three basic showings. First, there must be some suggestion or motivation, either in the references or in the

prior knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. (*See, e.g.*, In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Since the Examiner has failed to make the three basic showings, no *prima facie* case of obviousness has been established. Thus, claim 14 is improperly rejected under § 103(a) as being unpatentable over Wang in view of Shinohara. Claim 15 depends from claim 14 and is therefore improperly rejected for at least the same reasons.

4. Claims 2, 6, 11, and 14-15 Are Not Properly Rejected Under 35 U.S.C. § 103(a) as Being Unpatentable Over O'Neill in View of What is Well Known in the Art

(E) Claims 2, 6, and 11

Claim 2 depends from claim 1 and recites wherein the memory comprises an EEROM.

O'Neill and what is well known in the art do not, alone or in combination, disclose, teach, or suggest the claimed subject matter.

O'Neill is directed to "a software system and method for updating information which reduces the size of an update and distributes the update in a platform independent manner" (pg. 1, para. 0002 of O'Neill). In O'Neill, "an update generator . . . identifies differences between the updated operating code and the resident operating code and thereafter generates an update package comprising an instruction set which specifies how to generate the updated operating

code utilizing at least a portion of . . . the resident operating code" (pg. 2, para. 0013 of O'Neill). The update package is then distributed "to the electronic devices . . . and . . . executed by the client modules" residing thereon (pg. 2, para. 0013 of O'Neill).

(E)(i) Nothing well known in the art cures the deficiencies of O'Neill

Claim 2 depends from claim 1 and incorporates the limitations of that claim. As discussed above in Section (B)(i), O'Neill does not disclose, teach or suggest "providing information about the capabilities of the I/O connector panel to a memory within the I/O connector panel," as recited in claim 1.

The Examiner has not cited anything well known in the art as disclosing, teaching, or suggesting, "providing information about the capabilities of the I/O connector panel to a memory within the I/O connector panel," as recited in claim 1.

Therefore, even if O'Neill was combined with what is well known in the art, the combination would neither teach nor suggest "providing information about the capabilities of the I/O connector panel to a memory within the I/O connector panel," as recited in claim 1.

(E)(ii) The Examiner has not established a *prima facie* case of obviousness

To establish a *prima facie* case of obviousness, the Examiner must make three basic showings. First, there must be some suggestion or motivation, either in the references or in the prior knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim

limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. (*See, e.g.*, In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Since the Examiner has failed to make the three basic showings, no *prima facie* case of obviousness has been established. Thus, claim 2 is improperly rejected under § 103(a) as being unpatentable over O'Neill in view of what is well known in the art. Claims 6 and 11 each incorporates the features of claim 2 and are therefore improperly rejected for at least the same reasons.

(F) Claims 14-15

Claim 14 recites a processing system that includes a core PC function and a plurality of I/O connector panels coupled to the core PC function, each of the plurality of I/O connector panels comprising a plurality of I/O connectors, an EEROM containing information about the capabilities of the I/O connector panel, wherein, when the memory is examined, at least one driver can be downloaded to a system coupled to the I/O connector panel, and connector logic coupled to the EEROM for I/O distribution.

O'Neill and what is well known in the art do not, alone or in combination, disclose, teach, or suggest the claimed subject matter.

O'Neill is directed to "a software system and method for updating information which reduces the size of an update and distributes the update in a platform independent manner" (pg. 1, para. 0002 of O'Neill). In O'Neill, "an update generator . . . identifies differences between the updated operating code and the resident operating code and thereafter generates an update

package comprising an instruction set which specifies how to generate the updated operating code utilizing at least a portion of . . . the resident operating code" (pg. 2, para. 0013 of O'Neill). The update package is then distributed "to the electronic devices . . . and . . . executed by the client modules" residing thereon (pg. 2, para. 0013 of O'Neill).

(F)(i) O'Neill does not disclose, teach, or suggest "each of the plurality of I/O connector panels comprising . . . an EEROM containing information about the capabilities of the I/O connector panel"

O'Neill does not disclose, teach, or suggest "each of the plurality of I/O connector panels comprising . . . an EEROM containing information about the capabilities of the I/O connector panel," as recited in claim 14. In the final Office action, the Examiner states:

> O'Neill teaches . . . a plurality of I/O connector panels coupled to the core PC function, each of the plurality of I/O connector panels comprising a plurality of I/O connectors [e.g., fig. 1D; paragraph 0040], a memory containing information [server manifest in paragraphs 0048, 0057] about the capabilities [server manifest having a list or version information describing available update packages which pertain to a wide range of particular client devices attached to the update server array in paragraph 0048] of the I/O connector panel . . . .

(December 7, 2005 final Office action, pg. 8).

As discussed above in section (B)(i), construing the term "I/O connector panel" so broadly as to encompass a server or an array of servers is contrary to the interpretation that those skilled in the art would give. Under MPEP § 2111, "[t]he broadest reasonable interpretation of the claims must . . . be consistent with the interpretation that those skilled in the art would reach." In addition, as noted in section (D)(i) above, claim 14 explicitly distinguishes the "I/O connector panel" from a "core PC function" and a "system" by reciting that the "I/O connector panel" is coupled to both the "core PC function" and the "system." Thus, "server 136" and

"server array 142" in O'Neill cannot be construed as disclosing the "I/O connector panel" recited in claim 14.

Further, as discussed in section (B)(i) above, O'Neill also fails to disclose an "EEROM" in each "I/O connector panel" that contains "information about the capabilities of the I/O connector panel," as recited in claim 14, because "server 136" in O'Neill cannot be construed as disclosing the "I/O connector panel" recited in claim 14 and consequently, the "onboard memory or storage component" in server 136 cannot be construed as disclosing an "EEROM" in an "I/O connector panel" and the "server manifest" cannot be construed as disclosing "information about the capabilities of the I/O connector panel."

Therefore, O'Neill, like Wang, fails to disclose, teach, or suggest "each of the plurality of I/O connector panels comprising . . . an EEROM containing information about the capabilities of the I/O connector panel," as recited in claim 14.

(F)(ii) Nothing well known in the art cures the deficiencies of Wang

The Examiner has not cited anything well known in the art as disclosing, teaching, or suggesting, "each of the plurality of I/O connector panels comprising . . . an EEROM containing information about the capabilities of the I/O connector panel," as recited in claim 14.

Therefore, even if O'Neill was combined with what is well known in the art, the combination would neither teach nor suggest "each of the plurality of I/O connector panels comprising . . . an EEROM containing information about the capabilities of the I/O connector panel," as recited in claim 14.

(F)(iii) The Examiner has not established a *prima facie* case of obviousness

To establish a *prima facie* case of obviousness, the Examiner must make three basic showings. First, there must be some suggestion or motivation, either in the references or in the prior knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. (*See, e.g.*, In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Since the Examiner has failed to make the three basic showings, no *prima facie* case of obviousness has been established. Thus, claim 14 is improperly rejected under § 103(a) as being unpatentable over O'Neill in view of what is well known in the art. Claim 15 depends from claim 14 and is therefore improperly rejected for at least the same reasons.

CONCLUSION

On the basis of the above remarks, Appellant respectfully submits that the final rejection should be reversed.

Respectfully submitted,
SAWYER LAW GROUP LLP

Dated: May 4, 2006

Erin C. Ming
Attorney for Appellant(s)
Reg. No. 47,797
(650) 475-1449

APPENDIX OF CLAIMS

1. (Previously Presented) A method for automatically determining a configuration of an I/O connector panel, the method comprising:

providing information about the capabilities of the I/O connector panel to a memory within the I/O connector panel;

examining the information in the memory; and

downloading at least one driver to a system coupled to the I/O connector panel based upon the examined information.

2. (Original) The method of claim 1, wherein the memory comprises an EEROM.

3. (Original) The method of claim 1, wherein the downloading step is provided by software that is independent of the type of I/O connector panel.

4. (Original) The method of claim 1, wherein the system includes a core PC function block.

5. (Previously Presented) An I/O connector panel comprising:

a plurality of I/O connectors; and

a memory containing information about the capabilities of the I/O connector panel, wherein, when the memory is examined, at least one driver can be downloaded to a system coupled to the I/O connector panel.

6. (Original) The connector panel of claim 5 wherein the memory comprises an EEROM.

7. (Original) The connector panel of claim 5, wherein the system includes a core PC function block.

8. (Original) The connector panel of claim 5, further comprises connector logic coupled to the memory for I/O distribution.

9. (Original) The connector panel of claim 5, wherein the memory contains attributes of the I/O connector panel and attributes of each connector installed on the connector panel.

10. (Previously Presented) A processing system comprising:

a core PC function; and

at least one I/O connector panel coupled to the core PC function, the at least one I/O connector panel comprising: a plurality of I/O connectors and a memory containing information about the capabilities of the I/O connector panel, wherein, when the memory is examined, at least one driver can be downloaded to a system coupled to the I/O connector panel.

11. (Original) The processing system of claim 10, wherein the memory comprises an EEROM.

12. (Original) The processing system of claim 10, further comprises connector logic coupled to the memory for I/O distribution.

13. (Original) The processing system of claim 10, wherein the memory contains attributes of the I/O connector panel and attributes of each connector installed on the I/O connector panel.

14. (Previously Presented) A processing system comprising:

a core PC function; and

a plurality of I/O connector panels coupled to the core PC function, each of the plurality of I/O connector panels comprising a plurality of I/O connectors, an EEROM containing information about the capabilities of the I/O connector panel, wherein, when the memory is examined, at least one driver can be downloaded to a system coupled to the I/O connector panel, and connector logic coupled to the EEROM for I/O distribution.

15. (Original) The processing system of claim 14, wherein the memory contains attributes of the I/O connector panel and attributes of each connector installed on the I/O connector panel.